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QUESTION BANK

Subject with Code : DICD (16EC5703)   **Course & Branch**: M.Tech - VLSI

Year & Sem: I-M.Tech & I-Sem

UNIT –I

1. a) Draw the circuit for NMOS inverter and explain its operation.   5M

    b) Compare the characteristics of the different types of MOS inverters in terms of
        noise margin and power dissipation.   5M

2. a) What makes dynamic CMOS circuits faster than static CMOS circuits?   5M

    b) Draw the ideal characteristics of a CMOS inverter and compare it with the actual
        characteristics.   5M

3. Design a static CMOS circuit to realize the following functions:

    a) $F = b + (a \bullet c) + ca$.   5M

    b) XNOR gate.   5M

4. a) Draw the circuit topology and explain the operation of CMOS domino logic.   5M

    b) How clock skew problem is overcomes in domino CMOS circuits?   5M

5. a) Implement the 2-input NAND gate with CMOS logic and explain its working.   5M

    b) What are the advantages of dynamic logic over static CMOS logic?   5M

6. a) With the help of diagrams, explain about static CMOS inverter.   5M

    b) Discuss about the performance of dynamic CMOS inverter.   5M

7. a) Implement the 2-input NOR gate with static CMOS and dynamic CMOS.   5M

    b) How clock skew problem is overcome in NORA CMOS circuits?   5M

8. a) Construct a XNOR gate in dynamic logic and explain its working.   5M

    b) What are the problems associated with dynamic logic?   5M

9. a) How does the domino logic solves the problem in dynamic logic?   5M

    b) In which way NORA logic is power efficient? Explain with appropriate equations. 5M

10. a) Design 4-to-1 MUX using CMOS transmission gate.   5M

    b) Compare the sources of power dissipation between static CMOS and dynamic CMOS. 5M

UNIT-II

1. a) Illustrate the method of logical effort for transistor sizing.   5M

   b) Explain the read/write operation of the SRAM cell.   5M

2. Prove that the delay of a series of pass transistors can be reduced from quadratic dependence to

   linear dependence on the number of transistors in series by inserting buffers at suitable intervals.10M

3. a) Explain about different strategies for building low power CMOS gates.   5M

   b) Draw the circuit for 4 transistors SRAM and explain its working.   5M

4. a) Why low power has become an important issue in the present day VLSI circuit realization? 5M

   b) Explain how read and write operations are performed in a SRAM.   5M

5. a) Sketch the schematic diagram of a SRAM memory cell along with sense amplifier and

      data write circuitry.   7M

   b) Discuss about power consumption in CMOS gates.   3M

6. a) What is meant by logical effort?   4M

   b) Give the design considerations of a 4 bit SRAM with the help of CMOS logic diagram.   6M

7. a) Explain the logical effort of two – input NAND and NOR gates with neat circuit diagram.   6M

   b) In what way the DRAMs differ from SRAMs?   4M

8. a) Explain about different strategies for building low power CMOS gates.   5M

   b) Explain the read and write operations for a one transistor DRAM cell.   5M

9. a) Explain with a neat sketch about the operation of the 6 transistor SRAM cell.   5M

   b) Explain the design considerations of a 4 bit RAM with the help of CMOS logic diagram.   5M

10. a) What is short circuit power dissipation? On what parameters does it depend?   5M

    b) Draw one cell dynamic RAM circuit and explain its working.   5M

UNIT-III

1. What is dynamic behavior of BiCMOS logic? Explain in detail with neat sketches.   10M

2. Give the schematic diagram of different Bi-CMOS inverters. Explain its operation.   10M

3. a) Compare the switching characteristics of a BiCMOS inverter with respect to that for static

    CMOS for different fan out conditions.   5M

  b) Design NAND gate in BiCMOS logic.   5M

4. a) Explain how to calculate the delay for the BiCMOS circuits.   5M

  b) Explain the concept of BiCMOS inverter.   5M

5. Explain in detail how do we calculate power for BiCMOS and on what parameters

    the power equation depends on?   10M

6. Draw and explain the static and dynamic characteristics of BICMOS inverter.   10M

7. a) Discuss about delay and power consumption in BICMOS logic circuits.   5M

  b) List the advantages and disadvantages of BiCMOS.   5M

8. Explain the working principle of BiCMOS with the help of static and dynamic characteristics. 10M

9. Explain about bipolar gate design in detail with neat sketches.   10M

10. What is static behavior of BiCMOS logic? Explain in detail with neat sketches.   10M

UNIIT-IV

1. a) What are the general observations on the design rules?   5M

   b) Write about NMOS based design rules.   5M

2. a) Discuss about 'Mead Conway Design' rules for silicon gate NMOS process.   6M

   b) What is the need for design rules? Explain.   4M

3. Design a CMOS logic gates for the function $F = \overline{(A + BC)D}$. Also indicate the connections of signals F, VDD and GND. Draw the stick diagram representation for the circuit designed.   10M

4. a) What are the CMOS based design rules?   4M

   b) Explain two input NAND gate with relevant Layout example.   6M

5. Draw the stick diagram for the following schematic using appropriate colors.   10M
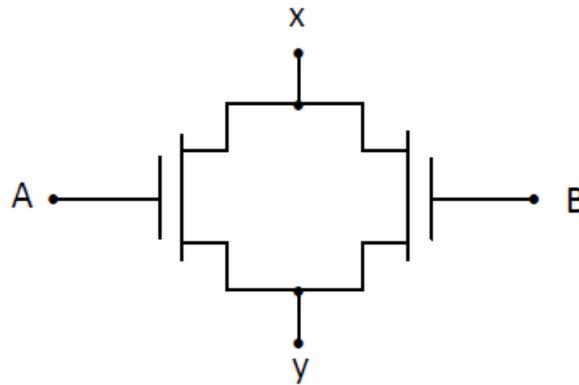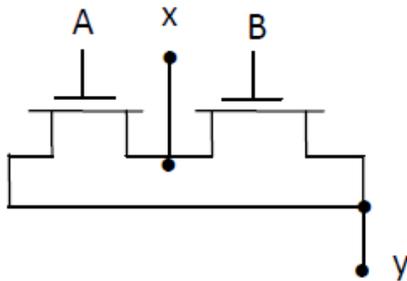
6. Write about:

   (i) Area capacitance.   5M

   (ii) Drive large capacitive load.   5M

7. a) What is the need of wired capacitance? Where it is used? Explain.   5M

   b) What is area capacitance? Explain its significance in the layout design.   5M

8. Write about:

   (i) Sheet resistance.   5M

   (ii) Lambda based design rules.   5M

9. a) What is sheet resistance? Find out the expression f_o the resistance of rectangular sheet in terms of sheet resistance.   5M

   b) Find out the capacitance of a MOS capacitor.   5M

10. a) Implement the 2-input XOR gate for CMOS logic and explain its working.   5M

    b) Design Layout Diagram for above diagram with relevant colors.   5M

UNIT-V

1. a) How to design a 4-bit shifter? Explain with schematic. 5M

   b) What is pipeline multiplier array? Explain. 5M

2. a) Discuss about design approach of carry look ahead adder with neat sketch. 5M

   b) Explain Booth's algorithm and its modified algorithm. 5M

3. a) Compare different types of CMOS subsystem shifters. 5M

   b) Discuss about design approach of 4 bit shifter. 5M

4. a) Draw and explain the booth decode cell used for booth multiplier. 5M

   b) Design a 4 bit CLA adder. 5M

5. a) Analyze the timing of this 4 bit CLA. 5M

   b) Compare CLA with RCA and state its merits and demerits. 5M

6. a) Draw the circuit diagram of 4 bit Baugh-Wooley multiplier structure and explain. 5M

   b) Comment on the advantages and disadvantages of the multiplier. 5M

7. a) How to design the ALU sub-system? Give the process. 5M

   b) Design the sub-system Serial Parallel Multiplier. 5M

8. a) Analyze the timing of the array multiplier. 5M

   b) Explain the modified booth algorithm. 5M

9. a) Construct 4-bit SISO and explain its operations. 5M

   b) With a neat sketch explain the working of array multiplier. 5M

10. a) Design the circuit diagram of logarithmic shifter using CMOS logic. 5M

    b) Explain what is subsystem design process. 5M

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